What is claimed is:

1. A device comprising:

a plurality of data transceivers for transferring input data and output data;

a plurality of write strobe transceivers for transferring timing information of the input data and for transferring a first group of auxiliary information;

a plurality of read strobe transceivers for transferring timing information of the output data and for transferring a second group of auxiliary information; and

an auxiliary circuit connected to the data transceivers and the write and read strobe transceivers for generating the first group of auxiliary information.

2. The device of claim 1, wherein the auxiliary circuit includes an inversion controller for conditionally inverting the input and output data.

3. The device of claim 2, wherein the auxiliary circuit further includes a parity controller for generating a parity code of the output data.

4. The device of claim 3, wherein the auxiliary circuit further includes a temperature reporter for generating temperature information of the device.

5. The device of claim 4, wherein the auxiliary circuit further includes a calibrator for calibrating a timing of a transfer of the output data.

6. The device of claim 1, wherein the write strobe transceivers include at least one write strobe receiver connected to the auxiliary circuit for transferring the second group of auxiliary information to the auxiliary circuit.

7. The device of claim 6, wherein the read strobe transceivers include at least one read strobe transmitter connected to the auxiliary circuit for transferring the first group of auxiliary information from the auxiliary circuit.

8. A device comprising:

a memory array for receiving inbound data and for outputting outbound data;

an input data path for transferring the inbound data to the memory array;

an output data path for transferring the outbound data from the memory array;

a plurality of data transceivers for transferring input data to the input path as the inbound data and for transferring the outbound data from the output path as output data;

a plurality of write strobe transceivers for transferring timing information of the input data and for transferring a first group of auxiliary information;

a plurality of read strobe transceivers for transferring timing information of the output data and for transferring a second group of auxiliary information; and

an auxiliary circuit connected to the data transceivers and the write and read strobe transceivers for generating the first group of auxiliary information.

9. The device of claim 8, wherein the auxiliary circuit includes an inversion controller for conditionally inverting the input and output data.

10. The device of claim 9, wherein the auxiliary circuit further includes a parity controller for generating a parity code of the output data.

11. The device of claim 10, wherein the auxiliary circuit further includes a temperature reporter for generating temperature information of the memory device.

12. The device of claim 11, wherein the auxiliary circuit further includes a calibrator for calibrating a timing of a transfer of the output data.

13. The device of claim 8, wherein the write strobe transceivers include at least one write strobe receiver connected to the auxiliary circuit for transferring the second group of auxiliary information to the auxiliary circuit.

14. The device of claim 13, wherein the read strobe transceivers include at least one read strobe transmitter connected to the auxiliary circuit for transferring the first group of auxiliary information from the auxiliary circuit.

15. A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a memory array for receiving inbound data and for outputting outbound data;

an input data path for transferring the inbound data to the memory array;

an output data path for transferring the outbound data from the memory array;

a plurality of data transceivers for transferring input data to the input path as the inbound data and for transferring the outbound data from output path as output data;

a plurality of write strobe transceivers for transferring timing information of the input data and for transferring a first group of auxiliary information;

a plurality of read strobe transceivers for transferring timing information of the output data and for transferring a second group of auxiliary information; and

an auxiliary circuit connected to the data transceivers and the write and read strobe transceivers for generating the first group of auxiliary information.

16. The system of claim 15, wherein the auxiliary circuit includes an inversion controller for conditionally inverting the input and output data.

17. The system of claim 16, wherein the auxiliary circuit further includes a parity controller for generating a parity code of the output data.

18. The system of claim 17, wherein the auxiliary circuit further includes a temperature reporter for generating temperature information of the memory device.

19. The system of claim 18, wherein the auxiliary circuit further includes a calibrator for calibrating a timing of a transfer of the output data.

20. The system of claim 15, wherein the write strobe transceivers include at least one write strobe receiver connected to the auxiliary circuit for transferring the second group of auxiliary information to the auxiliary circuit.

21. The system of claim 20, wherein the read strobe transceivers include at least one read strobe transmitter connected to the auxiliary circuit for transferring the first group of auxiliary information from the auxiliary circuit.

22. A method of transferring data in a device, the method comprising:
transferring timing information of data via a first set of transceivers;
transferring the data via data transceivers; and
transferring auxiliary information via a second set of strobe transceivers, wherein transferring the auxiliary information occurs during transferring of the timing information.

23. The method of claim 22, wherein transferring auxiliary information includes transferring input inverting code.

24. The method of claim 23, wherein transferring auxiliary information includes transferring input parity code.

25. The method of claim 24, wherein transferring auxiliary information includes transferring temperature code.

26. The method of claim 25, wherein transferring auxiliary information includes transferring calibrating code.

27. The method of claim 22, wherein transferring timing information including transferring timing information of data inputted to the device.

28. The method of claim 22, wherein transferring timing information including transferring timing information of data outputted from the device

29. A device comprising:

a plurality of data transceivers for transferring input data and output data, the output data being generated based on outbound data;

a plurality of write strobe transceivers for transferring timing information of the input data and for transferring an input inverting code;

a plurality of read strobe transceivers for transferring timing information of the output data and for transferring an output inverting code; and

an inversion controller connected to the data transceivers and the write and read strobe transceivers for conditionally inverting the input data and for conditionally inverting the outbound data.

30. The device of claim 29, wherein the inversion controller includes:

a calculating unit for generating the output inverting code based on the outbound data; and

an inverting unit for inverting the outbound data based on the output inverting code and for inverting the input data based on the input inverting code.

31. The device of claim 30, wherein the read strobe transceivers include at least one read strobe transmitter connected to the inversion controller for transferring the output inverting code.

32. The device of claim 31, wherein the write strobe transceivers include at least one write strobe receiver connected to the inversion controller for transferring the input inverting code.

33. The device of claim 29, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

34. The device of claim 29, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

35. A memory device comprising:

a memory array for receiving inbound data and for outputting outbound data;

an input data path for transferring the inbound data to the memory array;

an output data path for transferring the data from the memory array;

a plurality of data transceivers for transferring input data to the input path as the inbound data and for transferring the outbound data from output path as output data;

a plurality of data transceivers for transferring input data and output data, the output data being generated based on outbound data;

a plurality of write strobe transceivers for transferring timing information of the input data;

a plurality of read strobe transceivers for transferring timing information of the output data; and

an inversion controller connected to the data transceivers and the write and read strobe transceivers for conditionally inverting the input data and for conditionally inverting the outbound data.

36. The memory device of claim 35, wherein the read strobe transceivers include at least one read strobe transmitter connected to the inversion controller for transferring the output inverting code.

37. The memory device of claim 36, wherein the write strobe transceivers include at least one write strobe receiver connected to the inversion controller for transferring the input inverting code.

38. The memory device of claim 35, wherein the inversion controller includes an inverting unit connected between the data transceivers and the input and output data path.

39. The memory device of claim 38, wherein the inverting unit includes a plurality of first switching devices, each of the first switching devices includes:

an inverter connected between one of the data transceivers and the input path; and

a switch connected around the inverter for allowing data to bypass the inverter based on the input inverting code.

40. The memory device of claim 39, wherein the inverting unit further includes a plurality of second switching devices, each of the second switching devices includes:

an inverter connected between one of the data transceivers and the output path; and

a switch connected around the inverter for allowing data to bypass the inverter based on the output inverting code.

41. The memory device of claim 38, wherein the inversion controller further includes a calculating unit for generating the output inverting code based on the outbound data.

42. The memory device of claim 41, wherein the calculating unit includes a comparing portion for comparing the outbound data of a first output cycle with the outbound data of a second output cycle.

43. The memory device of claim 35, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

44. The memory device of claim 35, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

45. A system comprising:

a processor; and

a memory device connected to the processor, the memory device includes:

an input data path for transferring inbound data to the memory array;

an output data path for transferring the outbound data from the memory array;

a plurality of data transceivers for transferring input data to the input path as inbound data and for transferring the outbound data from output path as output data;

a plurality of data transceivers for transferring an input data and an output data, the output data being generated based on an outbound data;

a plurality of write strobe transceivers for transferring timing information of the input data;

a plurality of read strobe transceivers for transferring timing information of the output data; and

an inversion controller connected to the data transceivers and the write and read strobe transceivers for conditionally inverting the input data and for conditionally inverting the outbound data.

46. The system of claim 45, wherein the inversion controller includes:

a calculating unit for generating the output inverting code based on the outbound data; and

an inverting unit for inverting the outbound data based on the output inverting code and for inverting the input data based on the input inverting code.

47. The system of claim 45, wherein the read strobe transceivers include at least one read strobe transmitter connected to the inversion controller for transferring the output inverting code.

48. The system of claim 45, wherein the write strobe transceivers include at least one write strobe receiver connected to the inversion controller for transferring the inverting code.

49. The system of claim 45, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

50. The system of claim 45, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

51. A method of transferring data in a device, the method comprising:

transferring timing information of data via a first set of transceivers;

transferring the data via data transceivers; and

transferring an inverting code via a second set of strobe transceivers, wherein transferring the inverting code occurs during the transferring of the timing information.

52. The method of claim 51, wherein transferring the data includes transferring input data to the device.

53. The method of claim 52, wherein transferring the inverting code includes transferring an output inverting code associated with output data transferred from the device.

54. The method of claim 51, wherein transferring the data includes transferring output data from the device.

55. The method of claim 54, wherein transferring the inverting code includes transferring an input inverting code associated with input data transferred to the device.

56. A device comprising:

a plurality of data transceivers for transferring input data and output data;

a plurality of write strobe transceivers for transferring timing information of the input data and for receiving an input parity code of the input data;

a plurality of read strobe transceivers for transferring timing information of the output data and for transferring an output parity code of the output data; and

a parity controller connected to the data transceivers and the write and read strobe transceivers for generating the output parity and for verifying the input data based on the input parity code.

57. The device of claim 56, wherein the parity controller includes:

a parity generator for generating the output parity code based on the output data and for generating a calculated input parity code based on the input data; and

a verifier for verifying the input data based on the calculated input parity and the input parity code.

58. The device of claim 57, wherein the read strobe transceivers include at least one read strobe transmitter connected to the parity controller for transferring the output parity code.

59. The device of claim 58, wherein the write strobe transceivers include at least one write strobe receiver connected to the parity controller for transferring the input parity code.

60. The device of claim 56, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

61. The device of claim 56, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

62. A memory device comprising:

a memory array for receiving inbound data and for outputting outbound data;

an input data path for transferring the inbound data to the memory array;

an output data path for transferring the data from the memory array;

a plurality of data transceivers for transferring input data to the input path as the inbound data and for transferring the outbound data from output path as output data;

a plurality of data transceivers for transferring input data and output data, the output data being generated based on outbound data;

a plurality of write strobe transceivers for transferring timing information of the input data;

a plurality of read strobe transceivers for transferring timing information of the output data; and

a parity controller connected to the data transceivers and the write and read strobe transceivers for generating the output parity and for verifying the input data based on the input parity code.

63. The memory device of claim 62, wherein the parity controller includes an output parity unit connected to the data transceivers for generating the output parity code based on the output data, and connected to the read strobe transceivers for providing the output parity code to the read strobe transceivers.

64. The memory device of claim 63, wherein the parity controller further includes the input parity unit connected to the data transceivers for generating a calculated input parity code based on the input data.

65. The memory device of claim 64, wherein the parity controller further includes a comparator for comparing the input parity code and the calculated input parity code.

66. The memory device of claim 62, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

67. The memory device of claim 62, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

68. A system comprising:

a processor; and

a memory device connected to the processor, the memory device includes:

an input data path for transferring inbound data to the memory array;

an output data path for transferring the outbound data from the memory array;

a plurality of data transceivers for transferring input data to the input path as inbound data and for transferring the outbound data from output path as output data;

a plurality of data transceivers for transferring input data and output data, the output data being generated based on an outbound data;

a plurality of write strobe transceivers for transferring timing information of the input data;

a plurality of read strobe transceivers for transferring timing information of the output data; and

a parity controller connected to the data transceivers and the write and read strobe transceivers for generating the output parity and for verifying the input data based on the input parity code.

69. The system of claim 68, wherein the parity controller includes:

a parity generator for generating the output parity code based on the output data and for generating a calculated input parity code based on the input data; and

a verifier for verifying the input data based on the calculated input parity and the input parity code.

70. The system of claim 69, wherein the read strobe transceivers include at least one read strobe transmitter connected to the parity controller for transferring the output parity code.

71. The system of claim 70, wherein the write strobe transceivers include at least one write strobe receiver connected to the parity controller for transferring the input parity code.

72. The system of claim 68, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

73. The system of claim 68, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

74. A method of transferring data in a device, the method comprising:
transferring timing information of data via a first set of transceivers;
transferring the data via data transceivers; and
transferring a parity code via a second set of strobe transceivers, wherein transferring the parity code occurs during the transferring of the timing information.

75. The method of claim 74, wherein transferring the data includes transferring input data to the device.

76. The method of claim 75, wherein transferring the parity code includes transferring an output parity code associated with output data transferred from the device.

77. The method of claim 74, wherein transferring the data includes transferring output data from the device.

78. The method of claim 77, wherein transferring the parity code includes transferring an input parity code associated with input data transferred to the device.

79. A device comprising:

a plurality of data transceivers for transferring input data and output data;

a plurality of write strobe transceivers for transferring timing information of the input data;

a plurality of read strobe transceivers for transferring timing information of the output data and for transferring temperature information; and

a temperature reporter connected to the write and read strobe transceivers for generating the temperature information of the device.

80. The device of claim 79, wherein the temperature reporter includes:

a temperature sensor for sensing a temperature of the device to produce a temperature information; and

a temperature output circuit to output the temperature information.

81. The device of claim 80, wherein the temperature output circuit includes:

a signal converter for converting the temperature information into digital temperature data; and

a format converter for converting the digital temperature data to a serial format.

82. The device of claim 79, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

83. The device of claim 79, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

84. A memory device comprising:

a memory array for receiving inbound data and for outputting outbound data;

an input data path for transferring the inbound data to the memory array;

an output data path for transferring the data from the memory array;

a plurality of data transceivers for transferring input data to the input path as the inbound data and for transferring the outbound data from output path as output data;

a plurality of data transceivers for transferring an input data and an output data, the output data being generated based on an outbound data;

a plurality of write strobe transceivers for transferring timing information of the input data;

a plurality of read strobe transceivers for transferring timing information of the output data and for transferring temperature information; and

a temperature reporter connected to the write and read strobe transceivers for generating the temperature information of the memory device.

85. The memory device of claim 84, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

86. The memory device of claim 84, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

87. The memory device of claim 84, wherein the temperature reporter includes:

a temperature sensor for sensing a temperature of the memory device to produce a temperature information; and

a temperature output circuit to output the temperature information.

88. The memory device of claim 87, wherein the temperature output circuit includes:

a signal converter for converting the temperature information into digital temperature data; and

a format converter for converting the digital temperature data to a serial format.

89. A system comprising:

a processor; and

a memory device connected to the processor, the memory device includes:

an input data path for transferring inbound data to the memory array;

an output data path for transferring the outbound data from the memory array;

a plurality of data transceivers for transferring input data to the input path as inbound data and for transferring the outbound data from output path as output data;

a plurality of data transceivers for transferring input data and output data, the output data being generated based on an outbound data;

a plurality of write strobe transceivers for transferring timing information of the input data;

a plurality of read strobe transceivers for transferring timing information of the output data and for transferring temperature information; and

a temperature reporter connected to the write and read strobe transceivers for generating the temperature information of the memory device.

90. The system of claim 89, wherein the temperature reporter includes:

a temperature sensor for sensing a temperature of the system to produce a temperature information; and

a temperature output circuit to output the temperature information.

91. The system of claim 90, wherein the temperature output circuit includes:

a signal converter for converting the temperature information into digital temperature data; and

a format converter for converting the digital temperature data to a serial format.

92. The system of claim 89, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

93. The system of claim 89, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

94. A method of transferring data in a device, the method comprising:

transferring timing information of data via a first set of transceivers;

transferring the data via data transceivers; and

transferring a temperature code via a second set of strobe transceivers, wherein transferring the temperature code occurs during the transferring of the timing information.

95. The method of claim 94, wherein transferring the data includes transferring input data to the device.

96. The method of claim 94, wherein transferring the temperature code includes transferring multiple temperature code bits representing the temperature of the device.

97. The method of claim 96, wherein transferring the parity code includes transferring an input parity code associated with input data transferred to the device.

98. A device comprising:

a plurality of data transceivers for transferring input data and output data;

a plurality of write strobe transceivers for transferring timing information of the input data and for transferring a calibrating code;

a plurality of read strobe transceivers for transferring timing information of the output data; and

a calibrator connected to the data transceivers and the write and read strobe transceivers for adjusting a timing of a transfer of the output data based on the calibrating code.

99. The device of claim 98, wherein the calibrator includes:

a calibrating code receiver connected to the write and read transceivers for receiving a calibrating code associated with a timing delay; and

a storage unit for storing the timing delay.

100. The device of claim 99, wherein the calibrator includes:

a converter for converting the calibrating code to a parallel format; and

a decoder for decoding the calibrating code to provide the timing delay.

101. The device of claim 98, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

102. The device of claim 98, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

103. A memory device comprising:

a memory array for receiving inbound data and for outputting outbound data;

an input data path for transferring the inbound data to the memory array;

an output data path for transferring the data from the memory array;

a plurality of data transceivers for transferring input data to the input path as the inbound data and for transferring the outbound data from output path as output data;

a plurality of data transceivers for transferring input data and output data, the output data being generated based on outbound data;

a plurality of write strobe transceivers for transferring timing information of the input data and for transferring a calibrating code;

a plurality of read strobe transceivers for transferring timing information of the output data; and

a calibrator connected to the data transceivers and the write and read strobe transceivers for adjusting a timing of a transfer of the output data based on the calibrating code.

104. The memory device of claim 103, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

105. The memory device of claim 103, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a

receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

106. The memory device of claim 103, wherein the calibrator includes:

a calibrating code receiver connected to the write and read transceivers for receiving a calibrating code associated with a timing delay; and

a storage unit for storing the timing delay.

107. The memory device of claim 106, wherein the calibrator includes:

a converter for converting the calibrating code to a parallel format; and

a decoder for decoding the calibrating code to provide the timing delay.

108. A system comprising:

a processor; and

a memory device connected to the processor, the memory device includes:

an input data path for transferring inbound data to the memory array;

an output data path for transferring the outbound data from the memory array;

a plurality of data transceivers for transferring input data to the input path as inbound data and for transferring the outbound data from output path as output data;

a plurality of data transceivers for transferring input data and output data, the output data being generated based on an outbound data;

a plurality of write strobe transceivers for transferring timing information of the input data and for transferring a calibrating code;

a plurality of read strobe transceivers for transferring timing information of the output data; and

a calibrator connected to the data transceivers and the write and read strobe transceivers for adjusting a timing of a transfer of the output data based on the calibrating code.

109. The system of claim 108, wherein the calibrator includes:

a calibrating code receiver connected to the write and read transceivers for receiving a calibrating code associated with a timing delay; and

a storage unit for storing the timing delay.

110. The system of claim 109, wherein the calibrator includes:

a converter for converting the calibrating code to a parallel format; and

a decoder for decoding the calibrating code to provide the timing delay.

111. The system of claim 108, wherein each of the data transceivers, each of the write strobe transceivers, and each of the read strobe transceivers include identical circuit elements.

112. The system of claim 108, wherein each of the data transceivers includes a receiver and a transmitter, each of the write strobe transceivers includes a receiver and a transmitter, and each of the read strobe transceivers includes a receiver and a transmitter.

113. A method of transferring data in a device, the method comprising:

transferring timing information of data via a first set of transceivers;

transferring the data via data transceivers; and

transferring a calibrating code via a second set of strobe transceivers, wherein transferring the calibrating code occurs during the transferring of the timing information.

114. The method of claim 113, wherein transferring the data includes transferring output data to the device.

115. The method of claim 114, wherein transferring the calibrating code includes transferring multiple calibrating code bits representing a timing delay.